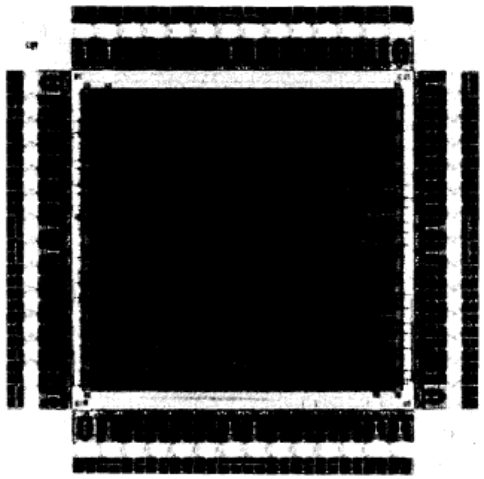
EXHIBIT X

Exhibit 16 - Hoefflinger

'156 Patent

Claim Limitation (Claim 7)	Exemplary Disclosure
[**156a**] A device comprising:	Hoefflinger's, *Digital Logarithmic CMOS Multiplier For Very-High-Speed Signal Processing*, discloses a device. *See, e.g.*: "The transistor count of a DIGILOG multiplier can be less than one quarter and the multiplication time can be less than one half in comparison with a Booth-Wallace multiplier." Hoefflinger, *Digital Logarithmic CMOS Multiplier For Very-High-Speed Signal Processing* at 16.7.1. "The microphotograph in figure 10 shows an experimental 8x8 bit multiplier with 10 bit logarithmic representation and a 16 bit output. It has been mapped on a two-micron semicustom GATE FOREST [5]. Its implementation required 800 transistors, and the multiplication time is 8 typical gate delays of the two micron CMOS process." Hoefflinger, *Digital Logarithmic CMOS Multiplier For Very-High-Speed Signal Processing* at 16.7.3.  Figure 10: Microphoto of semicustom test chip

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Claim Limitation (Claim 7)	Exemplary Disclosure
[**156b**] at least one first low precision high dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	Hoefflinger discloses at least one first low precision high dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See, e.g.*: "This process of logarithmic coding and decoding can be achieved with just two gate delays: One for obtaining the segments, a second one to obtain the outputs from the switch matrix." Hoefflinger, *Digital Logarithmic CMOS Multiplier For Very-High-Speed Signal Processing* at 16.7.2. "Logarithmic compression is used to handle signals with a wide dynamic range. PCM speech coding is the best example for this technique. The relative accuracy or, in other words, the maximum signal-to-noise ratio can be significantly less than the dynamic range. The latter is whereas the relative accuracy can be <8 bit equivalent to more than 12 bit." Hoefflinger, *Digital Logarithmic CMOS Multiplier For Very-High-Speed Signal Processing* at 16.7.2 "The segment signals are fed to the gates of the switch matrix shown in figure 5. The original bits a; are the inputs to this switch matrix and the outputs 12, 11 and 10 are obtained by passing through just one path transistor." Hoefflinger, *Digital Logarithmic CMOS Multiplier For Very-High-Speed Signal Processing* at 16.7.2.

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	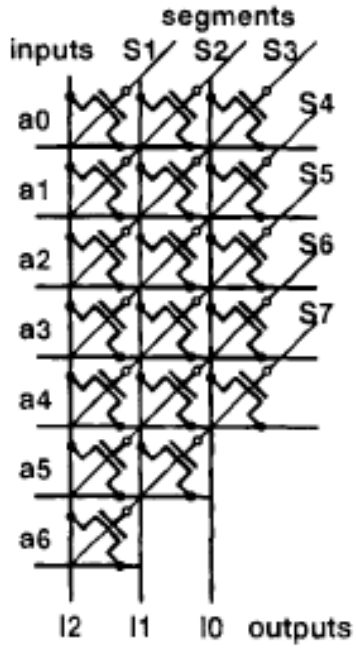 Figure 5: Switch matrix for 8 Bit lin to 6 Bit log encoder "The DIGILOG processing approach presented here enables high-resolution or wide-dynamic-range processing with limited word length. Besides its basic effectiveness, it thus provides an interesting compromise between fixed-point and floating-point processing systems." Hoefflinger, *Digital Logarithmic CMOS Multiplier For Very-High-Speed Signal Processing* at 16.7.3.
[**156c**] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first	Hoefflinger discloses the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical

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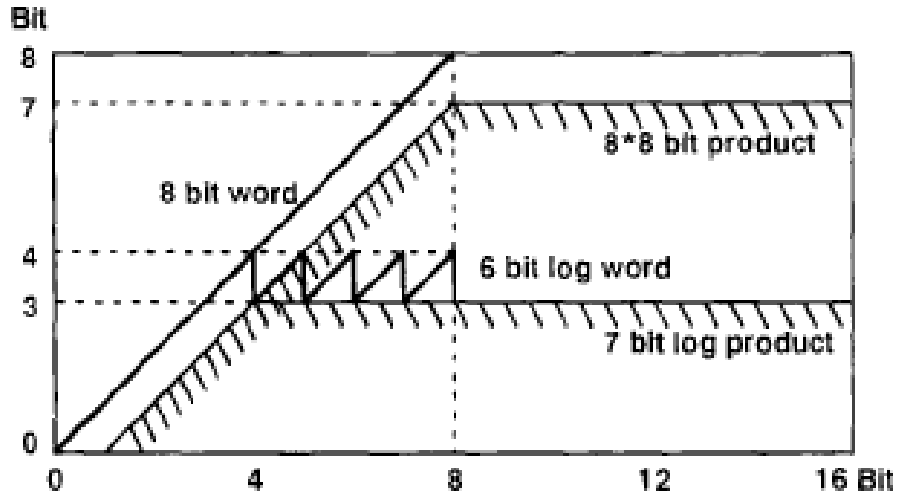
Claim Limitation (Claim 7)	Exemplary Disclosure
operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input; and	calculation of the first operation on the numerical values of that same input. *See, e.g.*: "Logarithmic compression is used to handle signals with a wide dynamic range. PCM speech coding is the best example for this technique. The relative accuracy or, in other words, the maximum signal-to-noise ratio can be significantly less than the dynamic range. The latter is whereas the relative accuracy can be <8 bit equivalent to more than 12 bit." Hoefflinger, *Digital Logarithmic CMOS Multiplier For Very-High-Speed Signal Processing* at 16.7.2 "[T]he logarithm of an originally 8 bit long word. In other words, dynamic range equivalent to 8 bits is compressed to a 6 bit logarithmic representation. The price for this is that the relative accuracy is not greater than 4 bit or 6 %. Nevertheless, for the lower half of the dynamic range on the logarithmic scale, the accuracy tracks that of the original representation. The diagram of figure 9 shows these properties of logarithmic compression." Hoefflinger, *Digital Logarithmic CMOS Multiplier For Very-High-Speed Signal Processing* at 16.7.2  Figure 9: Relative accuracy vs. signal level

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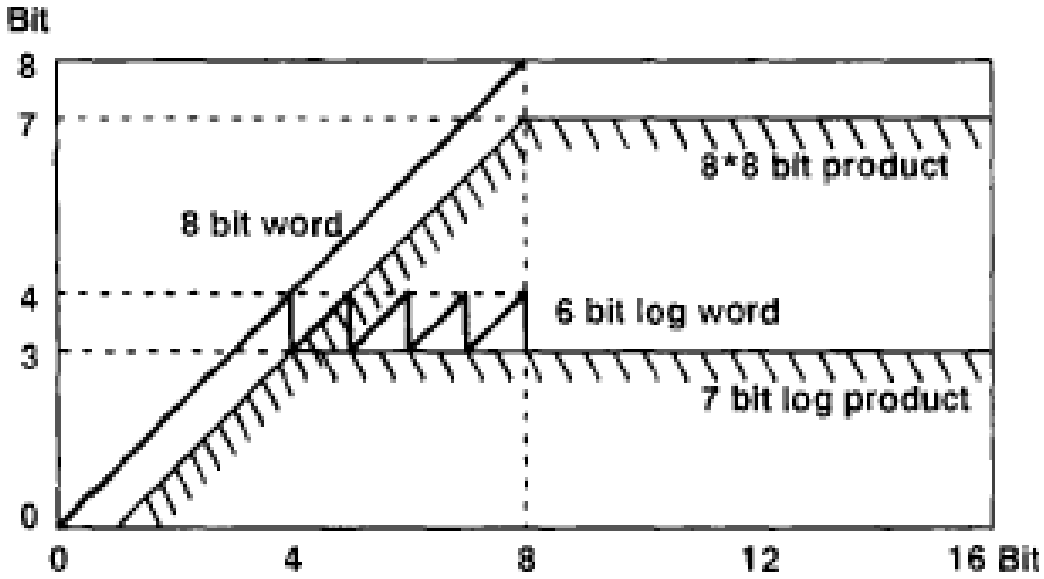
Claim Limitation (Claim 7)	Exemplary Disclosure
	"An abbreviated truth table of an 8x8 bit logarithmic multiplier is shown in figure 8. A multiplication result will be in one of 16 segments at one of 16 levels within that segment. A 4 bit relative accuracy is obtained for the result in our example. This accuracy is maintained over the upper dynamic range of 12 bit for a total dynamic range of 16 bit. A 7 bit logarithmic representation is readily expanded to cover a 16 bit dynamic range. This interesting property of Hoefflinger, *Digital Logarithmic* multiplication is also illustrated in figure 9, which shows the relative accuracy in bits as a function of the signal level in bits." Hoefflinger, *Digital Logarithmic CMOS Multiplier For Very-High-Speed Signal Processing* at 16.7.2.  Figure 9: Relative accuracy vs. signal level *See also* John N. Mitchell, Jr , *Computer Multiplication and Division Using Binary Logarithms*, IRE Transactions On Electronic Computers, 512-17 (Aug. 1962) (detailing error analysis for multiplication operations with LNS formats).

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Claim Limitation (Claim 7)	Exemplary Disclosure
[**156d**] at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit;	Hoefflinger discloses at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit. *See, e.g.*: "This process of logarithmic coding and decoding can be achieved with just two gate delays: One for obtaining the segments, a second one to obtain the outputs from the switch matrix." Hoefflinger, *Digital Logarithmic CMOS Multiplier For Very-High-Speed Signal Processing* at 16.7.2. To the extent that Singular contends that Hoefflinger does not itself identify a controller, notwithstanding this disclosure, a controller would have been obvious based on Hoefflinger alone or in combination with other disclosed prior art, including without limitation Lee, Belanovic, GRAPE-3, and Cray T3d, for the reasons explained in the Responsive Contentions.
[**156e**] wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine;	To the extent that Singular contends that Hoefflinger does not itself identify one of the disclosed computing devices, notwithstanding this disclosure, use of said computing device would have been obvious based on Hoefflinger alone or in combination with other disclosed prior art, including without limitation Lee, Belanovic, GRAPE-3, and Cray T3d, for the reasons explained in the Responsive Contentions.
[**156f**] and, wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.	Hoefflinger discloses the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide. *See, e.g.*: "There is an increasing interest in real-time signal processing in systolic arrays, in neural network implementations and in mathematical operations to put many, possibly hundreds, of multipliers on a single application-specific chip" Hoefflinger, *Digital Logarithmic CMOS Multiplier For Very-High-Speed Signal Processing* at 16.7.1.

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Claim Limitation (Claim 53)	Exemplary Disclosure
[**273a**] A device:	Hoefflinger discloses a device. *See* [**156a**].
[**273b**] comprising at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	Hoefflinger discloses at least one first low precision high dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See* [**156b**].
[**273c**] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X % of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;	Hoefflinger discloses the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input. *See* [**156c**]; *see also* Appendix to Responsive Contentions (detailing error rates associated with different input formats).
[**273d**] wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.	Hoefflinger discloses the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide. *See* [**156f**].

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Claim Limitation (Claim 4)	Exemplary Disclosure
[**961a**] A device comprising:	Hoefflinger's, *Digital Logarithmic CMOS Multiplier For Very-High-Speed Signal Processing*, discloses a device. *See* [**156a**].
[**961b**] at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	Hoefflinger discloses at least one first low precision high dynamic range (LPHDR) execution unit adapted to execute a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See* [**156b**].
[**961c**] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=10% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.2% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input; and	Hoefflinger discloses the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=10% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.2% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input. *See* [**156c**]; *see also* Appendix to Responsive Contentions (detailing error rates associated with different input formats).
[**961d**] at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit.	Hoefflinger discloses at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit. *See* [**156d**].

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Claim Limitation (Claim 13)	Exemplary Disclosure
[**961e**] A device comprising:	Hoefflinger discloses a device. *See* [**961a**]
[**961f**] a plurality of components comprising:	Hoefflinger discloses a plurality of components. *See* [**961b**] + **[961d**].
[**961g**] at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	Hoefflinger discloses at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See* [**961b**].
[**961h**] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=10% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.2% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input.	Hoefflinger discloses the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=10% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.2% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input. *See* [**156c**]; *see also* Appendix to Responsive Contentions (detailing error rates associated with different input formats).